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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/745,969	12/21/2000	Qiang Wu	4239010689	8506

7590 04/22/2004

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EXAMINER	
PERILLA, JASON M	

ART UNIT	PAPER NUMBER
2634	6

DATE MAILED: 04/22/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/745,969	WU ET AL.	
	Examiner	Art Unit	
	Jason M Perilla	2634	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *23 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-14,19 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,6,7,19,21 and 23* is/are rejected.

7)☒ Claim(s) *8-14* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 December 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 4, 6-14, 19, and 21-23 are pending in the instant application.

Claim Objections

2. Claim 10 recites the limitation "the predetermined threshold" in line 4. There is insufficient antecedent basis for this limitation in the claim.

3. Regarding claim 19, it is suggested that the limitation of "ceasing to consider the data once the input signal is detected" of line 7 is replaced by --ceasing to consider the tracked data once the input signal is detected— to maintain consistency in the claim.

4. Regarding claim 22, it is suggested that the limitation including "the tracked data is for a period at least as long as the latency period" of line 2 is replaced by --the step of tracking data continues ~~tracked data is~~ for a period at least as long as the latency period" --.

Claim Rejections

5. The indicated allowability of claims in the first office action is withdrawn in view of the newly discovered reference(s) to Hamlin et al. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 23, 6, and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Hamlin et al.

Regarding claim 23, Hamlin et al discloses a digital signal processor comprising: an analog front end (col. 1, lines 50-55) including an analog-to-digital converter for receiving an input signal (col. 1, lines 60-63); a digital base-band processor (col. 1, lines 50-55) having a latency period (inherent) for detecting a signal, coupled to the analog front end (col. 4, lines 12-19); a first shift register (fig. 1, ref. 22; fig. 3, refs. 40 and 50) and a second shift register (fig. 1, ref. 22; fig. 3, refs. 40 and 50) for tracking data representing the relative amplitude of samples of the input signal (fig. 2, ref. 29; col 7, lines 54-67; fig. 3, refs. 40, 50;col. 9, lines 25-44); a gain control counter controlled by a current relative amplitude of sample of the input signal and an output from the shift registers (figs. 1 and 2, ref. 22 and 24), coupled to the shift registers (fig. 2, ref. 33); and a gain control circuit coupled to the counter for controlling gain of the input signal (fig. 1, ref. 30). The gain control counters disclosed by Halim et al are embodied in figure 1 as references 22 and 24. They comprise the first signal threshold detector and the second signal threshold detector, respectively, and each contains a latching counter (i.e. fig. 2, ref. 29) comprised of shift registers and logic gates (fig. 3). Each gain control counter is controlled by a current relative amplitude of the input signal (fig. 2, ref. 13) and an output from the shift register or latching counter (fig. 2, ref. 29). The output of the latching counter (fig. 2, ref. 31) is a feedback signal to the gain controller via reference signal 33 of figure 2. Therefore, the gain control counters of Halim et al are controlled by a current input and an input from the shift register.

Regarding claim 6, Hamlin et al disclose the limitations of claim 23 as applied above. Further, Hamlin et al discloses that the first shift register (fig. 2, ref. 29) is coupled to a first comparator (fig. 2, ref. 26) which compares samples of the input signal with a lower threshold level (col. 7, lines 12-36).

Regarding claim 7, Hamlin et al disclose the limitations of claim 6 as applied above. Further, Hamlin et al discloses that the second shift register (fig. 2, ref. 29) is coupled to a second comparator (fig. 2, ref. 26) which compares samples of the sampled input signal with an upper threshold level (col. 7, lines 12-36). It is noted that the second threshold detector (fig. 1, ref. 24) is identical to the first threshold detector (fig. 1, ref. 22) and both the first and the second threshold detectors are shown by the same figures 2 and 3 although they each contain a separate comparator and shift register.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 1, 4, 19, 21, and 22are rejected under 35 U.S.C. 103(a) as being unpatentable over Halim et al (5036527) in view of Sutterlin et al (5463662).

Regarding claim 1, Halim et al discloses a digital signal processor comprising: an analog front end (col. 1, lines 50-55) including an analog-to-digital converter for receiving an input signal (col. 1, lines 60-63); a digital base-band processor (col. 1, lines

50-55) having a latency period (inherent) for detecting a signal, coupled to the analog front end (col. 4, lines 12-19); a shift register for tracking data representing the relative amplitude of samples of the input signal for a period at least equal to the latency period (fig. 2, ref. 29; col.7, lines 54-67; fig. 3, refs. 40, 50;col. 9, lines 25-44); a gain control counter (figs. 1 and 2, ref. 22 and 24), coupled to the shift register (fig. 2, ref. 33), controlled by a current relative amplitude of sample of the input signal (fig. 2, ref. 13) and an output from the shift register (fig. 2, ref. 31 via ref. 33); and, a gain control circuit coupled to the counter for controlling gain of the input signal (fig. 1, ref. 30). The gain control counters disclosed by Halim et al are embodied in figure 1 as references 22 and 24. They comprise the first signal threshold detector and the second signal threshold detector, respectively, and each contains a latching counter (i.e. fig. 2, ref. 29) comprised of shift registers and logic gates (fig. 3). Each gain control counter is controlled by a current relative amplitude of the input signal (fig. 2, ref. 13) and an output from the shift register or latching counter (fig. 2, ref. 29). The output of the latching counter (fig. 2, ref. 31) is a feedback signal to the gain controller via reference signal 33 of figure 2. Therefore, the gain control counters of Halim et al are controlled by a current input and an input from the shift register. Halim et al does not disclose the control of the gain counter ceasing once the base-band processor detects a signal of a predetermined threshold from the analog front end. However, Sutterlin et al does teach an automatic gain controller (AGC) wherein the gain of the AGC is halted in response to an input signal of a predetermined threshold being detected (fig. 8; col. 11, lines 10-25 and lines 27-33). Sutterlin et al teaches that the AGC is placed into a low-gain state

(gain control is ceased) in response to the detection of an input signal being above a predetermined threshold so that signal clipping is prevented. Therefore, it would have been obvious to one of ordinary skill in the art at the time which the invention was made to cease the operation of the AGC or the gain control counter in response to the detection of an input signal of a predetermined threshold as taught by Sutterlin et al in the digital signal processor of Hamlin et al because clipping of signals could be prevented due to a excessively large input signals.

Regarding claim 4, Hamlin et al in view of Sutterlin et al disclose the limitations of claim 1 as applied above. Further, Hamlin et al discloses that the gain control circuit includes a comparator for comparing a count in the gain control counter with a predetermined count and based upon the results of the comparison, adjusts the gain of the input signal (fig.1, ref. 30; col. 8, line 45-col. 9, line 21). The gain control circuit of Hamlin et al makes a comparison using the two inputs (fig. 1, refs. 31 and 32) taken from the first and second threshold detectors. These outputs from the first and second threshold detectors are created based upon the results of a comparison with a predetermined count (col. 8, lines 8-19). Hence, the gain of the input signal is adjusted based upon the comparison by the gain control counter of a predetermined count (col. 8, lines 58-61).

Regarding claim 19, Hamlin et al discloses a method for controlling gain in a digital signal processor comprising: tracking data representing the relative amplitude of an input signal (fig. 2, ref. 29; col.7, lines 54-67; fig. 3, refs. 40, 50;col. 9, lines 25-44); controlling the gain by considering a current amplitude and a prior amplitude from the

tracked data (figs. 1-3; col. 4, line 27-col. 6, line 2; col. 7, lines 14-36). Halim et al does not disclose ceasing to consider the tracked data once the input signal is detected. However, Sutterlin et al does teach an automatic gain controller (AGC) wherein the gain of the AGC is halted in response to an input signal being detected (fig. 8; col. 11, lines 10-25 and lines 27-33). Sutterlin et al teaches that the AGC is placed into a low-gain state (gain control is ceased) in response to the detection of an input signal being above a predetermined threshold so that signal clipping is prevented. Therefore, it would have been obvious to one of ordinary skill in the art at the time which the invention was made to cease the operation of the AGC or the gain control counter in response to the detection of an input signal of a predetermined threshold as taught by Sutterlin et al in the digital signal processor of Hamlin et al because clipping of signals could be prevented due to a excessively large input signals.

Regarding claim 21, Hamlin et al in view of Sutterlin et al disclose the limitations of claim 19 as applied above. Further, Hamlin et al discloses that the tracking step comprises, recording first bits representing samples of the input signal that exceed a first predetermined threshold (figs. 1 and 2, ref. 22; col. 7, lines 12-36) and second bits representing samples of the input signal that are less than a second predetermined threshold (figs. 1 and 2, ref. 24; col. 7, lines 12-36).

Regarding claim 22, Hamlin et al discloses the limitations of claim 21 as applied above. Further, Hamlin et al discloses that the processor has a signal detection latency period (inherent) and the step of tracking data continues for a period at least as long as the latency period. It is inherent that the processor will have a signal detection latency

period. In this case, it is also inherent that the step of tracking data continues at least as long as the latency period of signal detection because the processor is able to make at least one signal detection. Hence, the step of tracking data does continue longer than the latency period of the processor.

Allowable Subject Matter

10. Claims 8-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason M Perilla whose telephone number is (703) 305-0374. The examiner can normally be reached on M-F 8-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven Chin can be reached on (703) 305-4714. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Jason M Perilla
April 5, 2004

jmp

DETAILED ACTION

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Claim Objections

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3. Regarding claim 19, it is suggested that the limitation of "ceasing to consider the data once the input signal is detected" of line 7 is replaced by --ceasing to consider the tracked data once the input signal is detected— to maintain consistency in the claim.

4. Regarding claim 22, it is suggested that the limitation including "the tracked data is for a period at least as long as the latency period" of line 2 is replaced by --the step of tracking data continues ~~tracked data is~~ for a period at least as long as the latency period" --.

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Regarding claim 6, Hamlin et al disclose the limitations of claim 23 as applied above. Further, Hamlin et al discloses that the first shift register (fig. 2, ref. 29) is coupled to a first comparator (fig. 2, ref. 26) which compares samples of the input signal with a lower threshold level (col. 7, lines 12-36).

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(gain control is ceased) in response to the detection of an input signal being above a predetermined threshold so that signal clipping is prevented. Therefore, it would have been obvious to one of ordinary skill in the art at the time which the invention was made to cease the operation of the AGC or the gain control counter in response to the detection of an input signal of a predetermined threshold as taught by Sutterlin et al in the digital signal processor of Hamlin et al because clipping of signals could be prevented due to a excessively large input signals.

Regarding claim 4, Hamlin et al in view of Sutterlin et al disclose the limitations of claim 1 as applied above. Further, Hamlin et al discloses that the gain control circuit includes a comparator for comparing a count in the gain control counter with a predetermined count and based upon the results of the comparison, adjusts the gain of the input signal (fig.1, ref. 30; col. 8, line 45-col. 9, line 21). The gain control circuit of Hamlin et al makes a comparison using the two inputs (fig. 1, refs. 31 and 32) taken from the first and second threshold detectors. These outputs from the first and second threshold detectors are created based upon the results of a comparison with a predetermined count (col. 8, lines 8-19). Hence, the gain of the input signal is adjusted based upon the comparison by the gain control counter of a predetermined count (col. 8, lines 58-61).

Regarding claim 19, Hamlin et al discloses a method for controlling gain in a digital signal processor comprising: tracking data representing the relative amplitude of an input signal (fig. 2, ref. 29; col.7, lines 54-67; fig. 3, refs. 40, 50;col. 9, lines 25-44); controlling the gain by considering a current amplitude and a prior amplitude from the

tracked data (figs. 1-3; col. 4, line 27-col. 6, line 2; col. 7, lines 14-36). Halim et al does not disclose ceasing to consider the tracked data once the input signal is detected. However, Sutterlin et al does teach an automatic gain controller (AGC) wherein the gain of the AGC is halted in response to an input signal being detected (fig. 8; col. 11, lines 10-25 and lines 27-33). Sutterlin et al teaches that the AGC is placed into a low-gain state (gain control is ceased) in response to the detection of an input signal being above a predetermined threshold so that signal clipping is prevented. Therefore, it would have been obvious to one of ordinary skill in the art at the time which the invention was made to cease the operation of the AGC or the gain control counter in response to the detection of an input signal of a predetermined threshold as taught by Sutterlin et al in the digital signal processor of Hamlin et al because clipping of signals could be prevented due to a excessively large input signals.

Regarding claim 21, Hamlin et al in view of Sutterlin et al disclose the limitations of claim 19 as applied above. Further, Hamlin et al discloses that the tracking step comprises, recording first bits representing samples of the input signal that exceed a first predetermined threshold (figs. 1 and 2, ref. 22; col. 7, lines 12-36) and second bits representing samples of the input signal that are less than a second predetermined threshold (figs. 1 and 2, ref. 24; col. 7, lines 12-36).

Regarding claim 22, Hamlin et al discloses the limitations of claim 21 as applied above. Further, Hamlin et al discloses that the processor has a signal detection latency period (inherent) and the step of tracking data continues for a period at least as long as the latency period. It is inherent that the processor will have a signal detection latency

period. In this case, it is also inherent that the step of tracking data continues at least as long as the latency period of signal detection because the processor is able to make at least one signal detection. Hence, the step of tracking data does continue longer than the latency period of the processor.

Allowable Subject Matter

10. Claims 8-14 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

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Jason M Perilla
April 5, 2004

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